**AEC-Q102 Certification of Design, Construction and Qualification**

Supplier Name:       Date:

The following information is required to identify a part that has met the requirements of AEC-Q102. Submission of the required data in the format shown below is optional. **All entries must be completed; if a particular item does not apply, enter "Not Applicable".** This template can be downloaded from the AEC website at http://www.aecouncil.com.

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| **Item Name** | **Supplier Response** |
| 1. User’s Part Number: |       |
| 2. Supplier Part Number/Generic Part Number: |       |
| 3. Device Description: |       |
| 4. Wafer/Die Fab Location & Process ID:a. Facility name/plant #:b. Street address:c. Country: |                 |
| 5. Wafer Probe Location:a. Facility name/plant #:b. Street address:c. Country: |                 |
| 6. Assembly Location & Process ID:a. Facility name/plant #:b. Street address:c. Country: |                 |
| 7. Final Quality Control (Test) Location:a. Facility name/plant #:b. Street address:c. Country: |                 |
| 8. ESD-protective devicea. Manufacturer:b. Facility name/plant #: |            |
| 9. Wafer/Die:a. Wafer size:b. Die family:c. Die mask set revision & name: |                 |
| 10. Wafer/Die Technology Description:a. Wafer/Die process technology:b. Substrate materialc. Number of mask steps: |                 |
| 11. Die Dimensions:a. Die width:b. Die length:c. Die thickness (finished): |                 |
| 12. Die (frontside) Metallization:a. Die metallization material(s):b. Number of layers:c. Thickness (per layer):d. % of alloys (if present): |                      |
| 13. Die Passivation:a. Number of passivation layers:b. Die passivation material(s):c. Thickness(es) & tolerances: |                 |

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| 14. Die Overcoat Material  |       |
| 15. Die Prep Backside:a. Die prep method:b. Die metallization:c. Thickness(es) & tolerances: |                 |
| 16. Die Separation Method:a. Kerf width (μm):b. Kerf depth (if not 100% saw):c. Saw method: |           Single [ ]  Dual [ ]  |
| 17. Die Attach:a. Die attach material ID:b. Die attach method:c. Die placement diagram: |           See attached [ ]  Not available [ ]  |
| 18. Package:a. Type of package (e.g., plastic, ceramic, unpackaged):b. JEDEC designation (e.g. PLCC etc.): |            |
| 19. Mold Compounda. Mold compound supplier & ID:b. Mold compound type:1. Flammability rating:

d. Fire Retardant type/composition: e. Tg (glass transition temperature)(°C):f. CTE (above & below Tg)(ppm/°C): |           UL 94 V1 [ ]  UL 94 V0 [ ]            CTE1 (below Tg) =       CTE2 (above Tg) =       |
| 20 Encapsulation/Casting material:1. Encapsulation material supplier & ID:
2. Encapsulation material type:
3. Tg (glass transition temperature)(°C):
4. CTE (above & below Tg)(ppm/°C):
 |                          |
| 21. Wire Bond:a. Wire bond material:b. Wire bond diameter (mils): c. Type of wire bond at die:d. Type of wire bond at leadframe:e. Number of bonds over active area: |                           |
| 22. Leadframe:a. Leadframe material:b. Leadframe bonding plating composition:c. Leadframe bonding plating thickness (μinch):d. External lead plating composition:e. External lead plating thickness (μinch): f. External lead plating technology: |                                |
| 23. Board Material:1. Board material supplier & ID:
2. Board material type:
3. CTE:
 |                 |
| 24. Converter:1. Converter material supplier & ID:
2. Converter material type:
 |            |
| 25. Thermal Resistance:a. Junction - Ambient °C/W (approx):b. Junction - SolderJoint °C/W (approx): |            |
| 26. Maximum Process Exposure Conditions:a. MSL @ rated SnPb temperature:b. MSL @ rated Pb-free temperature:J-STD-020x fulfilled: | \* Note: Temperatures are as measured on the center of the plastic package body top surface.      at       °C (SnPb)      at       °C (Pb-free)[ ]  yes - revision:        [ ]  no |
| Attachments: |  | Requirements: |
| Die Photo | [ ]  | 1. A separate Certification of Design, Construction & Qualification must be submitted for each part number, wafer fab, and assembly location. |
| Package Outline Drawing | [ ]  |
| Die Cross-Section Photo/Drawing | [ ]  |
| Wire Bonding Diagram | [ ]  | 2. Design, Construction & Qualification shall be signed by the responsible individual at the supplier who can verify the above information is accurate and complete. Type name and sign below. |
| Die Placement Diagram | [ ]  |
| Completed by:       | Date: |       | Certified by:       | Date: |       |
| Typed or Printed: |       |       |
| Signature: |  |  |
| Title: |       |       |

This template is available as a stand-alone document that can be downloaded at

http://www.aecouncil.com.